Global Training Courses in Space Electronics

Combined Five-Day Programme

Time	Day 1	Day 2	Day 3	Day 4	Day 5
	Monday	**Tuesday**	**Wednesday**	**Thursday**	**Friday**
09:00	**FPGA 1** Space-grade FPGA technologies, COTS vs. Qualified, CMOS Scaling	**FPGA 5** Comparison of space-grade FPGAs implementing spacecraft IP	**Mixed Signal 1** Designing with ADCs : Understanding the ADC output spectrum	**Mixed Signal 5** Comparison of GSPS, broadband, space-grade ADC/DACs	**Power 1** Power distribution: DC-DCs, linear and switching POLs
10:30					
10:45	**FPGA 2** Space-grade SRAM, Flash & Antifuse FPGAs, fabrics, LUT vs. MUX, logic resources	**FPGA 6** System-level design: Clocking, powering FPGAs, power estimation, hardware debug	**Mixed Signal 2** Designing with DACs : Understanding the DAC output spectrum	**Mixed Signal 6** System-level design: Clocking, jitter and powering ADC/DACs	**Power 2** Comparison of space-grade, isolated DC-DCs. SiC vs. GaN vs. Si Power FETs, SEGR, SEB
12:15					
13:30	**FPGA 3** Radiation Hardness, SEE Mitigation & Reliability	**FPGA 7** High-speed serial links IBIS-AMI simulation BER Testing	**Mixed Signal 3** Dynamic Testing of ADCs and DACs	**Mixed Signal 7** Analogue front/back-end design and simulation Hyperlynx Analog & Linesim	**Power 3** Comparison of space-grade, linear and switching POLs
15:00					
15:15 16:45	**FPGA 4** FPGA vendors' design flows and software Xilinx Vivado/ISE Microsemi Libero Altera Quartus 2 Cobham/Atmel	**FPGA 8** PCB stack design, layout, design-for-EM, Signal & power integrity, power distribution networks and packaging	**Mixed Signal 4** RF ADCs/DACs, bandpass sampling, eliminating RF frequency conversion stages	**Mixed Signal 8** PCB stack design, layout, design-for-EMC, planes and analogue/digital partitioning. Post-layout simulation using Hyperlynx Analog and Boardsim	**Power 4** PCB stack design, layout, design-for-EMC, planes and current-carrying capacity
17:00	**Wrap Up**				

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